AgriCore: an agricultural application specific chip

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Abstract: As key executers of agricultural Internet of Things (IoT), the main control chip and abundance of applications are subjected to a wide variety of high energy-efficiency regulation. Designing application specific System-on-Chip (SoC) architecture underlying this regulation is critical for improving sensor data collection in the field of agricultural IoT. Targeting domain specific knowledge requires methods that can control all devices connected with both high performance and low power consumption. However, current agricultural IoT using chips directly from industry has hitherto been limited either by random selection and narrow functions, or by not considering environments. A SoC system of agricultural specific processor compatible with standard 8051 microcontroller instructions set was designed in this paper. The system uses a top-down approach, and Verilog HDL language to complete the design of memory cell, logic operation unit and other units in the chip integrated all logical circuits into the same function, and verify it on Xilinx FPGA. Part of the typical circuits has been tested through the implementation of the software simulation and verification of the peripheral circuits, and the test results show that the designed SoC system can be as expected to execute instructions and a FPGA development board debugging, and meet the design requirements. This relatively reasonable design can be manufactured using IP merge methods.

Keywords: SoC, agricultural IoT, FPGA, lower power consumption, 8051

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1 Introduction

Main control chip or Microcontroller Unit (MCU) has played a crucial role since the advent of agricultural informationization and agricultural Internet-of-Things (IoT). Whatever smart greenhouse or all kinds of sensors (Zhang et al., 2002) served for agricultural areas, when acquiring parameter data or other application data, the key executer will be the main control chip. The chips are likely involved in nearly all signal processing functions of the data collection devices as well as being altered in application specific units in the field of precision agriculture (Gebbers et al., 2010). A chip is manufactured from a silicon wafer, which is first cut to size and then etched with circuits and electronic devices. In the past several decades, all kinds of chips have achieved great success for improving the progress of human society. For example, the three types of mainstream chip are based upon ARM (Advanced RISC Machine), x86 and MIPS (millions of instructions per second) instruction set. Especially, as one of the most popular chips based on ARM architecture (Gong et al., 2013) has been widely used in many areas. However, these chips are mainly designed for industrial and consumer areas (Haight et al., 2016; Georgakopoulos et al., 2016; Wang et al., 2017; Ambrosin et al., 2016; Potyrailo et al., 2016; Cass et al., 2017), and few researchers have focused on agricultural areas. With the ever-increasing demand of agricultural

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IoT (Baranwal et al., 2016; Zou et al., 2017; Jin et al., 2015) and smart agriculture, the application specific chips (Bhongade et al., 2015; Cilardo et al., 2016; Knag et al., 2015) need to be designed to speed up the process of agricultural informationization.

In agricultural information areas, the application chips are mainly divided into two categories: one is for addressing problems in computer vision, image processing, speech recognition, UAV and robotics that can be hard to realize due to limited hardware capabilities, and the other is for application sensors, such as, CO_2, moisture, temperature and light intensity that mostly installed in smart greenhouses. Targeting more popular sensors requires methods that can acquire environment parameters with both high performance and low power consumption. This paper designs a SoC system (Menon et al., 2017) of agricultural specific processor compatible with standard 8051 microcontroller instructions set (Zheng et al., 2012; Chen et al., 2013; Hui et al., 2009). The system uses a top-down approach, and uses Verilog hardware description language (HDL) to complete the design of memory cell, logic operation unit and other units in the chip intergrated all the logical circuits with the same function, and verify it on Xilinx FPGA (Salim et al., 2006). Part of the typical circuits has been tested through the implementation of the software simulation and verification of the peripheral circuits, and the test results show that the designed SoC system can be as expected to execute instructions and a FPGA development board debugging, and meet the design requirements manufactured using IP merge methods.

2 Materials and method

2.1 Design flow

As one of the main drivers of the semiconductor technology in the past many years, System-on-Chip (SoC) contains digital, analog, mixed-signal, and other radio-frequency functions, integrated and employed intellectual property (IP) reuse to improve design productivity in an attempt to save costs and development time. Recently, designs of multi-million gate level with multiple third party IP cores have become commonplace. Efficient SoC designs based on IP reuse are implemented with hierarchical top-down design flows with previous designs done as IP used in the current design. In this paper, the design cycle as the diagram of SoC design flow is shown in Figure 1.

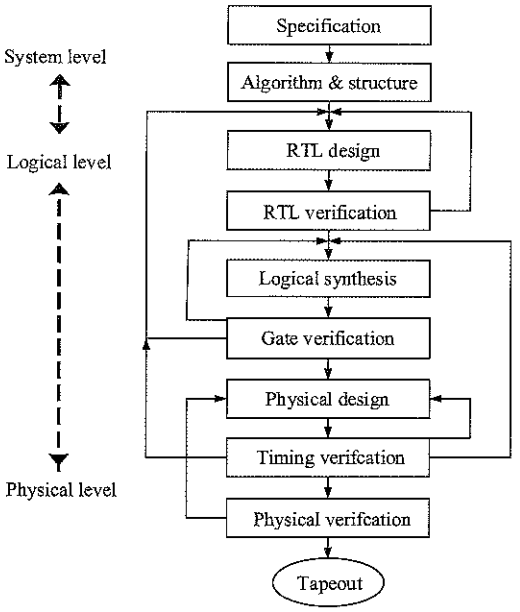

Figure 1 SoC design flow

There are three main stages: system level, logical level and physical level. Firstly, for system specification, designers should consider to refine architecture, algorithms; decompose into blocks; meet requirements and specifications; divide user interface, testing issues and applications. Furthermore, for logical implementation, register-transfer-language level (RTL) coding, IP integration, logical synthesis, verification and validation are inevitable. At the physical design phase, static and dynamic power consumption must be analyzed and power supply switches must be carefully placed, consequently, physical implementation will be acquired. Of course, the major bottlenecks are in the test and verification area. The system level and layout level links to RTL design play also an important role in a fluent design flow.

In accordance with the above design steps, in this paper presents an agricultural application specific chip named AgriCore that will provide services for agricultural informationization.

2.2 System structure and chip features

For sensor interface applied in agriculture, analog devices provide solutions to meet a wide range of automotive sensing challenges and improve vehicle

performance. The AgriCore instruction set is 100% compatible with the standard 8051 instruction set. It is particularly useful to designers who need the full ASIC top-level set of signals. The main on-chip modules are connected to the AgriCore by extending SFR (Special Function Registers) bus. The on-chip memory (including ROM and program and data RAM) is connected to the core via memory bus. The system structure is shown in Figure 2.

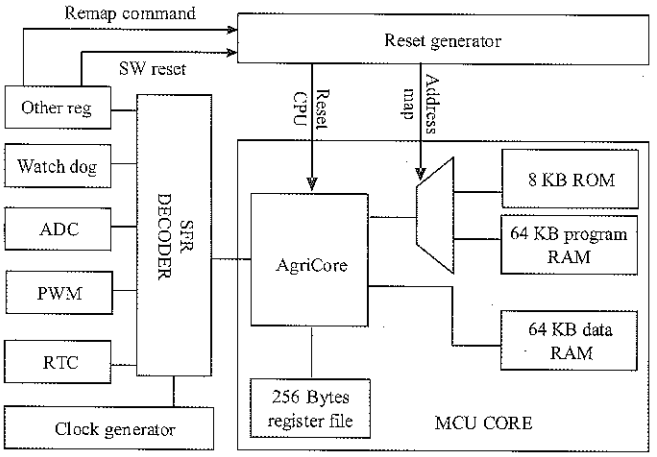

Figure 2 Diagram of the system structure

Features:

1) Compatibale with 8051 core;

2) Running frequency up to 120 MHz;

3) Configure phase locked loop (PLL);

4) ROM 8 KB;

5) 64 KB program RAM;

6) 64 KB data RAM;

7) Virtual Serial Peripheral interface SPI host interface to connect Flash chip;

8) 32 GPIO;

9) Three Timers;

10) Serial port of Universal Asynchronous Receiver/ Transmitter (UART);

11) 4 configurable PWM output;

12) 8 channel analog-to-digital converter (ADC);

13) Watchdog;

14) Real Time Clock;

15) The alternative to using external crystal (8 MHz) or internal LC oscillator (32 MHz) as a clock source;

16) Support a single 3.3 V power supply (built in LDO);

17) LQFP100 package.

2.3 IP cores reuse

For SoC design, the ideas of reuse and integration that will make SoC design and verification become simple. Well-specified cores interacting via clean and well-defined interfaces connected to the AgriCore in this paper played a critical role for improving the application. Figure 3 shows that the distribution of IP cores friendly intergrated into AgriCore and the base architecture is almost identical to the standard 8051, thus maintaining instruction-level compatibility. There are five IP cores existed the system: 1) S018ROSC_32MA: Mixed Signal 1.8V/3.3V Enhanced process Ring Oscillator 32 MHz single power supply: 1.8 V; 2) S018PLLGS_T500: Mixed Signal 1.8V/3.3V Enhanced process Clock Generator PLL, output freq. 25 M~500 MHz, with single power supply. Size: 621 um×265 um; 3) SP018_PX32K: Crystal Oscillator compatible with SP018, SP018W, SP018N; 4) S018AD2H: Mixed Signal 1.8V/3.3V Enhanced process 8-Channel 10bit 50K SAR ADC; 5) S018VREG18_ 150MCAP: This voltage regulator can provide up to 150 mA stable current with 1.8V +/-10% output voltage.

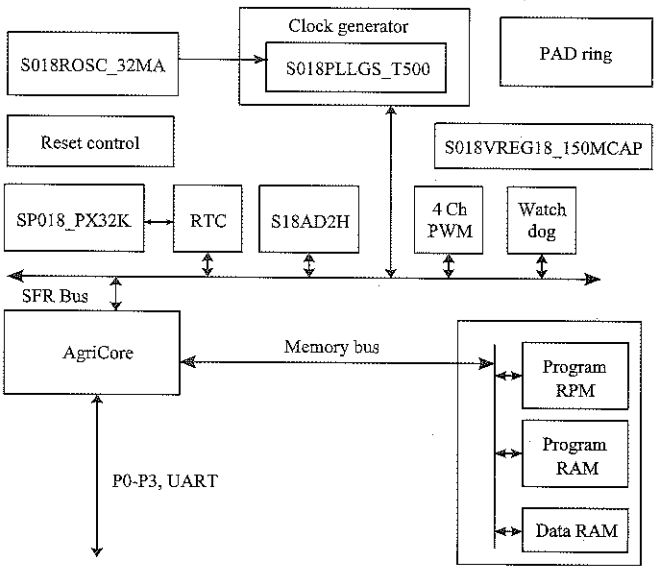

Figure 3 Diagram of IP core distribution

2.4 SFR registers

Standard 8051 has a fixed number of Special Function Registers (SFRs) defined. In AgriCore these fixed SFRs are all available; in addition, user can even add their own SFR in their design using this expansion port. For example, user can add more I/O port if the 4 I/O ports provided in AgriCore is insufficient. When compared to

memory mapped I/O devices, this method provides a much faster I/O access.

Special Function Registers (SFRs) are used by the 8051 as a quick method of accessing hardware. The standard 8051 has many SFRs for controlling the serial port, timers and I/O ports. In the AgriCore these registers are contained internal to the model. The designer can map in extra special function registers to the SFR space of the AgriCore, to control on-chip user specified hardware. The new SFRs must not conflict with the addresses of previously defined SFRs. Only the lowest 7 bits of the SFR address are brought out from the AgriCore, since by definition an SFR memory map occupies only addresses 0x80 to 0xFF. The Figures 4 and 5 are shown the waveforms of each module accessed through SFR bus.

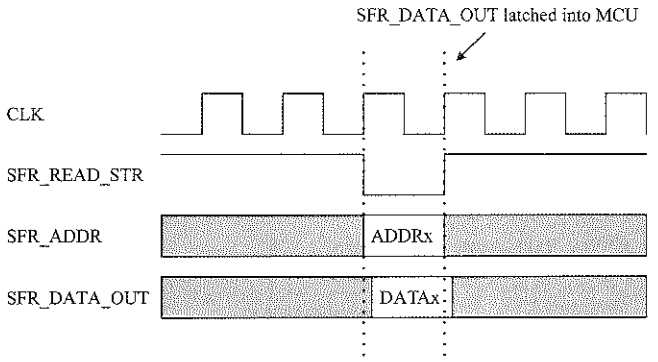

Figure 4 SFR read

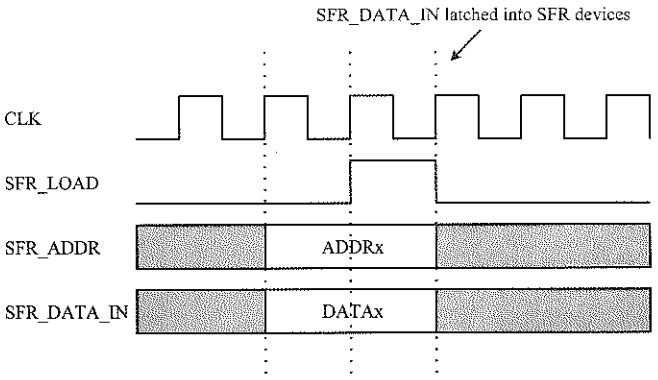

Figure 5 SFR write

2.5 Memory bus

The memory bus is the set of wires that is used to carry memory addresses and data to and from the system RAM. Alternatively, if the address on the program memory bus is checked when BusMon (0) is high, a record of program flow can be obtained. Similarly, a break point circuit can also be designed to detect if the program execution hit the breakpoint. The Figures 6 and 7 are shown the waveforms for accessing RAM/ROM through the Memory Bus module.

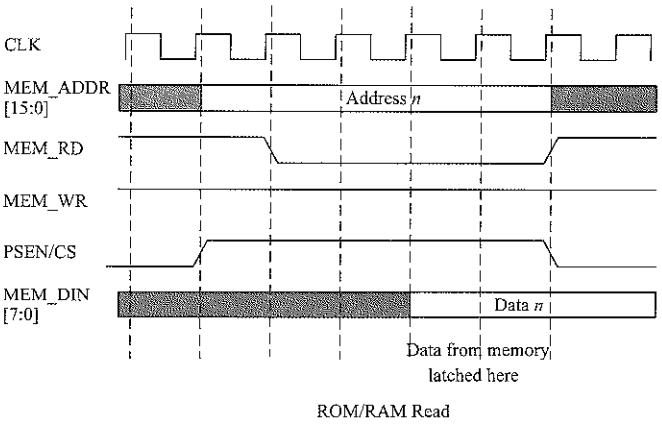

Figure 6 Memory bus read

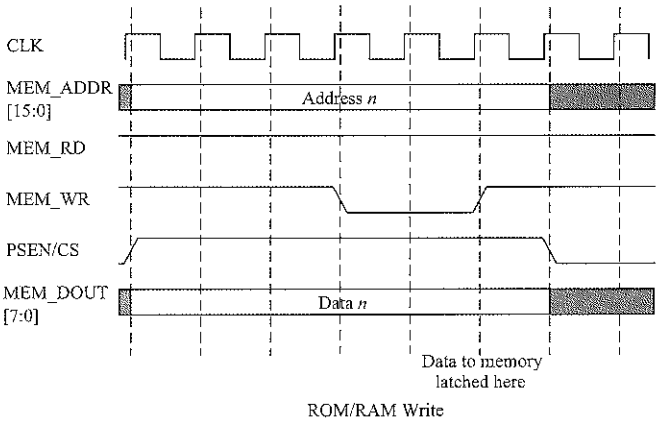

Figure 7 Memory bus write

2.6 Memory address mapping

One design goal of the AgriCore was to be able to use slow access time RAMs and ROMs with a fast processor. The standard 8051 performs two program memory fetches per machine cycle, but usually only uses the first one. In contrast, the AgriCore only does an extra program memory fetch during a jump. This means that for equivalent processing power, the AgriCore can use slower memories than the standard 8051. The memory bus of AgriCore can access three address ranges: startup ROM, program RAM, and data RAM. The 8KB startup ROM and program RAM using the address space, when the chip is powered on, AgriCore accesses the ROM space and executes the bootstrap program. At this time, 64KB program RAM space is mapped to the data RAM space to enable the software to be downloaded. At the end of the boot, AgriCore closes the ROM access space by configuring address mapping register and sets the address of program RAM and data RAM to a normal mapping relationship mode.

The extended SFR register address 0xEA is the address mapping control register REMAP [0]. When REMAP = 0, ROM is placed at the 0 address; when REMAP = 1, program RAM is placed at the 0 address. After the system reset, the value of REMAP returns to 0. When CPU is configured to be 1 through SFR bus, CPU subsystem reset will automatically trigger that enables CPU to start running from the 0x00 address of the REMAP.

Additionally, the chip uses free SFR address space to control major peripherals, such as Watchdog, ADC, etc.

2.7 Clock structure

The system has two clock sources: the 8MHz quartz oscillator and the resistance-capacitance (RC) oscillator. The quartz oscillator requires an external crystal. The internal RC oscillator eliminates the need for external crystals, but has relatively low clock accuracy. The selection of the two clock sources is controlled by the pin CLKSEL: the CLKSEL=1, using a crystal oscillator; the CLKSEL=0, using an internal RC oscillator. The internal RC oscillator generated about 32 MHz clock, and through frequency division using divide-by-2 produced about 8 MHz clock provided for PLL and directly drove core logic. In order to produce accurate baud rates in the UART boot mode, the external crystal oscillator should use the 11.0592 MHz frequency. The diagram clock structure is shown in Figure 8.

Although AgriCore has a machine cycle which is shorter than 12 cycles, in order to obtain compatibility with standard 8051 timers, the register is increased every 12 clock cycles when enabled in timer mode operation. And in counter mode operation, the register is incremented in response to falling edge at its corresponding external input pin, Timer 0, Timer 1, or Timer 2.

When the system started, the PLL is closed; if enable PLL to work, need to use the software register to generate required system clock.

Clock controller in the Clock Switch internal circuit is shown in Figure 9.

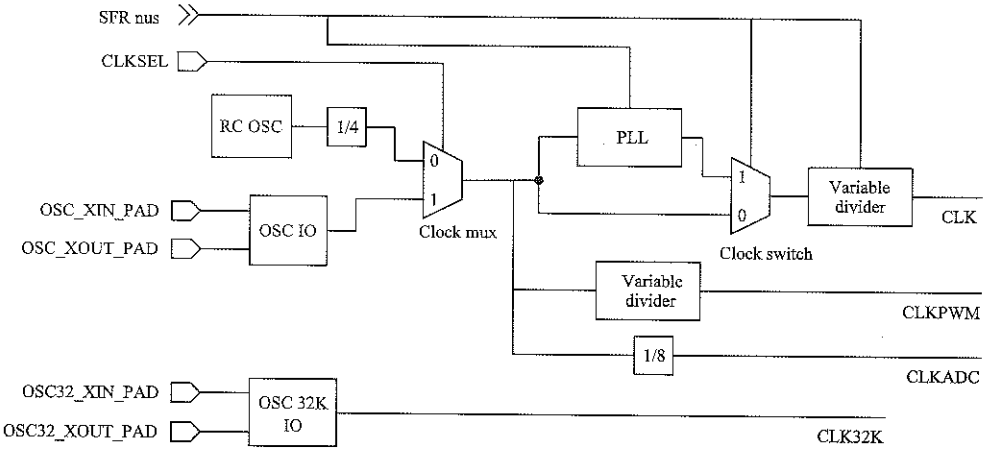

Figure 8 Clock structure

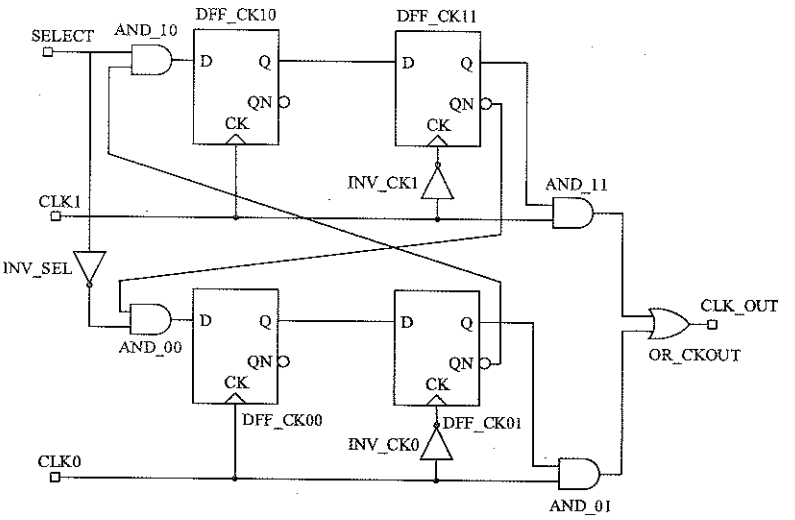

Figure 9 Clock Switch internal circuit

The SFR register used by the clock controller is listed below in Table 1.

Table 1 The SFR register used by the clock controller

SFR Address	Register	Reset Value	Descriptions
0xE9	SW_RESET	0x00	[0] – When write 1 to this bit, global chip reset will be triggered.
0xF1	CLKCFG	0x00	[7] - read only, CLKSEL pin status, 0 - uses internal 8MHz clock, 1 - uses external 11.0592MHz crystal clock [6] - PLL_SEL: 0 - uses the OSC clock as the main clock; 1 - uses the PLL output clock as the master clock [5:3] - PWM clock frequency division control: 0 - no divider 1 - 2 frequency division 2 - 4 frequency division ... 7 - 14 frequency division [2:0] - master clock frequency division control
0xF2	PLLCFG	0x17	[7] PLL_EN: 0 – PLL power down; 1 – PLL open [6:0] PLL frequency control: PLL output frequency = (Fosc * (2+PLLCFG))/8

2.8 Verification and testing

2.8.1 Verification in FPGA

On this board, the AgriCore is implemented inside a Xilinx FPGA. Since there is considerable spare capacity within the FPGA, used prototype the final on-chip logic within the FPGA also, allowing the full SoC to be prototyped in one FPGA and run at speed. To debug the embedded software, a simple software monitor has been developed. Figure 10 shows FPGA verification.

Figure 10 FPGA Verification

2.8.2 Flash read and write testing

The startup process of the chip is controlled by the program in the on-chip ROM. For AgriCore, the ROM program supports three functions:

Function 1: when connected to the PC through serial port, download the code to the program part of RAM, and jump to execute program.

Function 2: when connected to the PC through serial port, burn the code into the SPI Flash of the chip.

Function 3: without connecting to the PC, directly read the code from the outside SPI Flash, and put it into the program part of RAM, and jump to execute program.

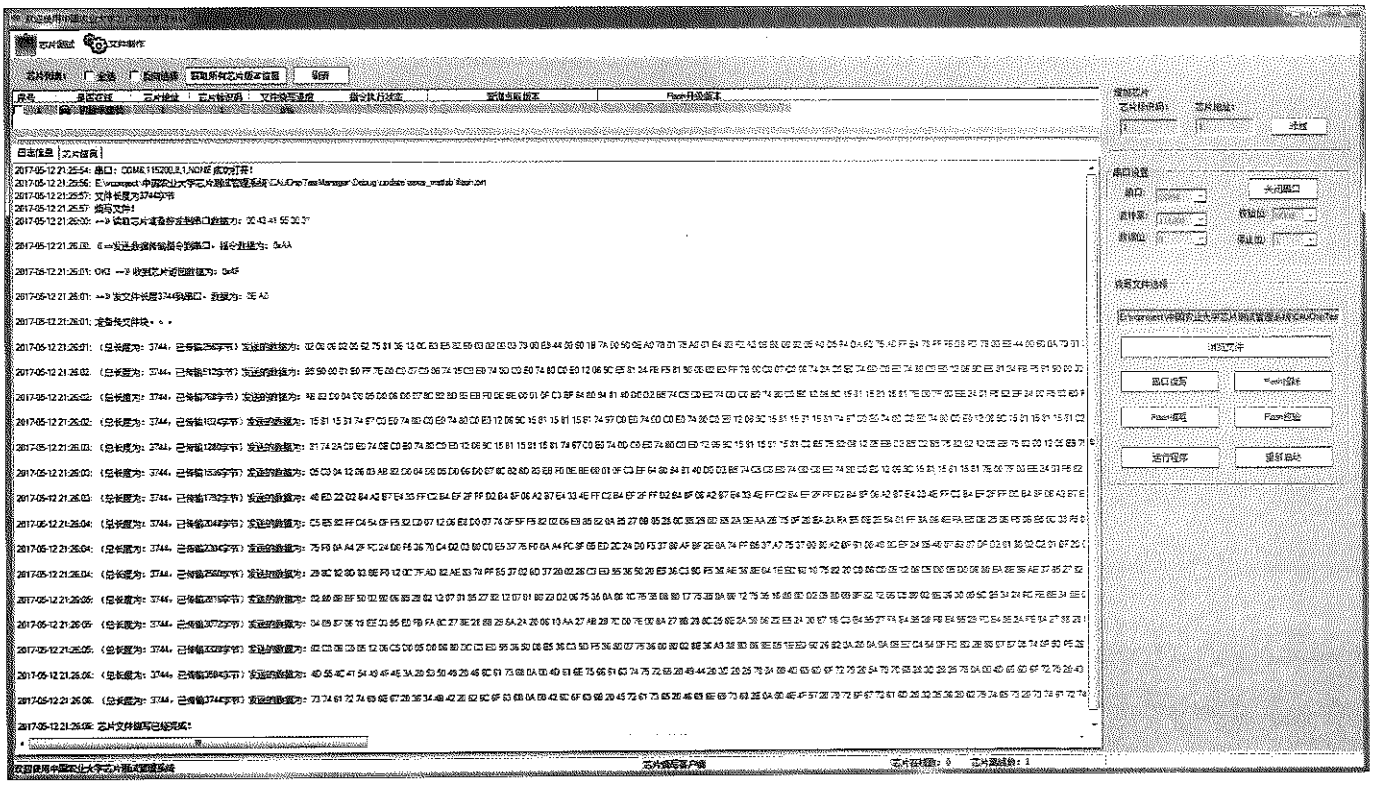

Figure 11 FLASH write and read

When the chip started, the chip will send the query string to the serial port, and if received the response from PC within a second, then finish Function 1 and Function 2 by an interactive command; if there is no response within one second, the Function 3 will be implemented and chip into the self-starting process. Figure 11 shows the process of embedded software written and read.

3 Results and discussion

The cell-based layout of based-AgriCore chip is shown in Figure 12. Through Synopsys software, the power of consumption of the chip is estimated as following Table 2. The total chip size is: the width is 4219.92, the height is 4219.92; and area is 17807724.81 μm^2.

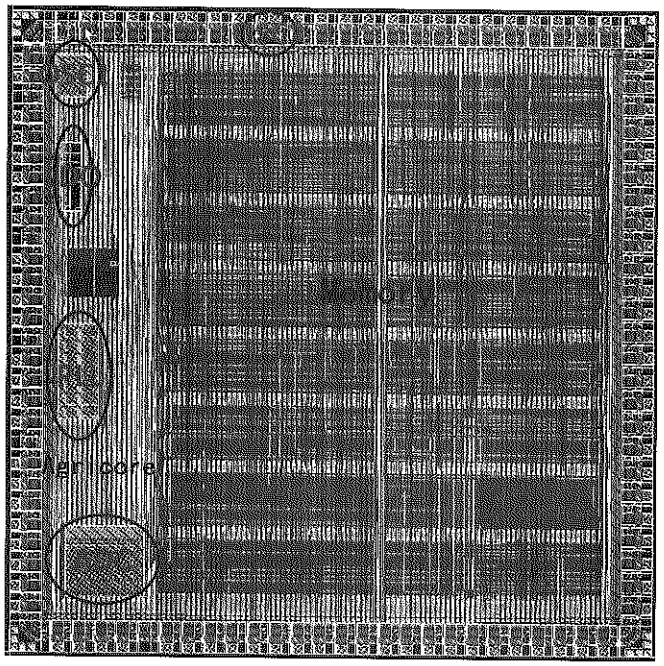

Figure 12 Snapshot of the layout

Table 2 Statistics for power consumption

units	Power, mW	(%)
Total Dynamic Power	15.2003	(100%)
Cell Internal Power	13.9765 mW	(92%)
Net Switching	1.2238 mW	(8%)
Dynamic Power	1	
Cell Leakage Power	0. 8050	

When applied in agricultural IoT areas for acquiring parameter values of soil moisture or air temperature, a smart sensor node based on AgriCore including four basic modules such as a power module, a sensing module, a processing module and a RF module which is shown in Figure 13. Sensing module mainly included sensor and ADC component, is connected to the processing module. The processing module can manage procedures through AgriCore to read data from sensor, and operate flash to store data. It also manages RF module which makes the sensor node join in the wireless sensor network. Of course, by this method, many applications can be implemented in different sensor nodes with relative interfaces.

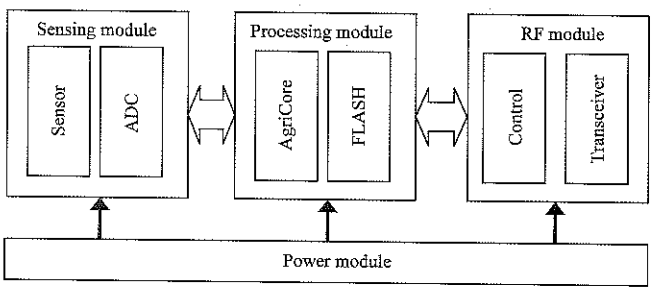

Figure 13 Modules of a smart sensor node based on AgriCore

4 Conclusions

The design methods of AgriCore SoC using chip development technology and the details of its implementation for rapid application in smart sensors of agricultural information areas were presented in this paper. The theoretical and empirical work in this paper demonstrates that SoC design method is an effective alternative to traditional methods to design a chip. In today's ARM-oriented MCU development environment, 8-bit devices might look old and a bit long, but in fact simple is the best. When coupled with modern process technologies and advanced mixed-signal peripherals, 8-bit performance on most control tasks can match or exceed many other CPU architectures, while providing improvements in speed, design time, size and integration. With the enhanced peripherals, these 8-bit machines can also offer a cost-effective solution that might preclude the need to move to a higher bus-width device, thus saving development time and money. The instruction execution in AgriCore is, on average, three times faster than standard part at the same clock frequency. In AgriCore, the Serial Transmission Clock is produced by the SerialClk and the transmission and reception of data are handled by SerialIn and SerialOut respectively. A tapeout schedule of the AgriCore chip is submitted.

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